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[54] ELECTRICALLY PROGRAMMABLE AND ERASABLE NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND OPERATING METHOD THEREFOR

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[56] References Cited

U.S. PATENT DOCUMENTS

4,173,791	11/1979	Bell
4,377,857	3/1983	Tickle
4,451,905	5/1984	Moyer
4,773,047	9/1988	Uchino et al. 365/181
4,868,619	9/1989	Mukherjee et al.
4,878,199	10/1989	Mizutani et al.

4,887,238	12/1989	Terasawa et al.
4,959,812	9/1990	Monodomi et al. 365/185.13
5,022,000	6/1991	Terasawa et al.
5,043,942	8/1991	Iwata et al. 365/189.01
5,077,691	12/1991	Haddad et al. 365/218
5,084,843	1/1992	Mitsuishi et al.
5,088,060	2/1992	Endoh et al.
5,126,808	6/1992	Montalvo et al.
5,197,027	3/1993	Challa
5,278,439	1/1994	Ma et al.
5,440,509	8/1995	Momodomi et al. 365/195
5,526,307	6/1996	Yiu et al. 365/185.01

FOREIGN PATENT DOCUMENTS

0422347A2	4/1991	European Pat. Off.
0429720A1	6/1991	European Pat. Off.
3831538A1	3/1989	Germany
1-282873	11/1989	Japan
2-3182	1/1990	Japan
3-295097	12/1991	Japan
4-14871	1/1992	Japan
5-6680	1/1993	Japan

OTHER PUBLICATIONS

"Experimental 4-Mb Flash EEPROM with Sector Erase", IEEE Journal of Solid-State Circuits, Mike McConnell, et al., vol. 26, No. 4, Apr. 1991, pp. 484-491.

"A 4-Mbit NAND-EEPROM with Tight Programmed Vt Distribution", Tanaka et al., 1990 Symposium on VLSI Circuits Digest of Technical Papers, pp. 105-106.

"A New Erasing and Row Decoding Scheme for Low Supply Voltage Operation 16 Mb/64-Mb Flash Memories", Miyawaki et al., IEEE Journal of Solid-State Circuits, vol. 27, No. 4, Apr. 1992, pp. 583-587.

(List continued on next page.)

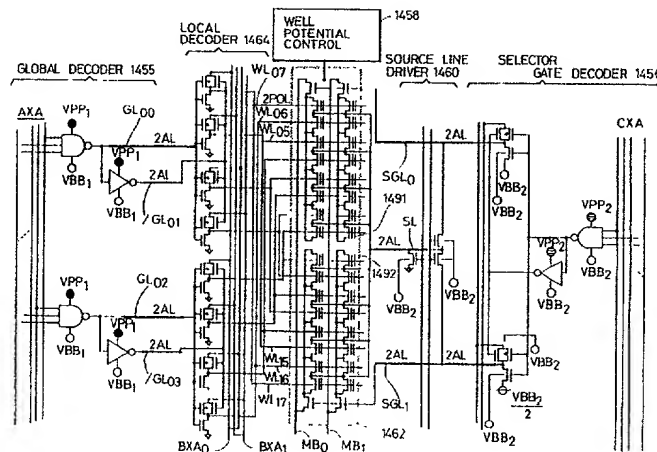
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[57] ABSTRACT

In erasing, electrons are simultaneously injected into floating gates from sources of a plurality of memory cells. Thus, the threshold voltages of the plurality of memory cells are increased. In programming, electrons are emitted from a floating gate of a selected memory cell to a drain. Thus, the threshold voltage of the selected memory cell is reduced.

2 Claims, 124 Drawing Sheets



OTHER PUBLICATIONS

"An Experimental 4-Mbit CMOS EEPROM with a NAND-Structured Cell", Momodomi et al., IEEE Journal of Solid-State Circuits, Vol. 24, No. 5., Oct. 1989, pp. 1238-1241.

"A High-Density NAND EEPROM with Block-Page Programming for Microcomputer Applications", IEEE Journal of Solid-State Circuits, Yoshihisa Iwata, et al., vol. 25, No. 2, Apr. 1990, pp. 417-424.

"An In-System Reprogrammable 32KX8 CMOS Flash Memory", Kynett et al., IEEE Journal of Solid-State Circuits, vol. 23, Nov. 5, Oct. 1988, pp. 1157-1163.

Nikkei Electronics, Feb. 17, 1992 (No. 547), pp. 180-181.

"A 3.42 μm^2 Flash Memory Cell Technology Conformable to a Sector Erase", Kume et al., 1991 Symposium on VLSI Technology, pp. 77-78.

"A 4-MB NAND EEPROM with Tight Programmed Vt Distribution", Momodomi et al., IEEE Journal of Solid-State Circuits, vol. 26, No. 4, Apr. 1991, pp. 492-495.

"A 5V Only 16Mbit Flash EEPROM Cell Using Highly Reliable Write/Erase Technologies", Kodama, et al., 1991 Symposium on VLSI Technology, pp. 75-76.

"An Asymmetrical Lightly Doped Source Cell for Virtual Ground High-Density EPROM's", Yoshikawa et al., IEEE Transactions on Electron Devices, vol. 37, No. 4, Apr. 1990, pp. 1046-1051.

Jacob Millman, Ph.D. et al. Microelectronics Second Edition, McGraw Hill Book Company, 1987, pp. 191-193.